AMENDMENTS

In the claims:

Please cancel claims 35 and 44. Please amend claims 36-39, 41-43, and 45-51 to read as follows:

36. (Amended) The method of claim 37, further comprising forming a second doped well within the first doped region, wherein forming the second doped plug includes forming the second doped plug in the second doped well a second distance from a boundary of the second n-well, and wherein the second distance is selected to provide approximately a desired resistance of a current path between the first doped plug and the second doped plug.

37. (Amended) A method, comprising:

providing a first doped region;

forming a first doped well within the first doped region;

forming a first doped plug within the first doped well, wherein the first doped plug is formed a first distance from a first boundary of the first doped well, and, wherein the first distance is selected to provide approximately a desired breakover voltage between the first doped plug and the first doped region;

forming a second doped plug into the first doped region; and

forming an isolation structure between the first and second doped plugs.

38. (Amended) The method of claim 37, wherein forming the isolation structure includes forming at least one of a LOCOS oxide and a surface trench filled with an oxide.

39. (Amended) The method of claim 37, wherein forming the isolation structure includes forming a gate terminal.

41. (Amended) The method of claim 37, further comprising forming a conductor layer above at least a portion of the first and second doped plugs.

42. (Amended) The method of claim 37, wherein providing the first doped region comprises providing a p-type first doped region.

43. (Amended) The method of claim 37, wherein forming the first and second doped plugs comprises forming n-type first and second doped plugs.

45. (Amended) The method of claim 46, further comprising forming a second n-well within the p-type semiconductor substrate, wherein forming the second n-plug within the p-type semiconductor substrate comprises forming the second n-plug within the second n-well a second distance from a boundary of the second n-well, and wherein the second distance is selected to provide approximately a desired resistance of a current path between the first n-plug and the second n-plug.

46. (Amended) A method comprising:

providing a p-type semiconductor substrate;

forming a first n-well within the p-type semiconductor substrate;

forming a first n-plug within the first n-well, wherein the first n-plug is formed a first distance from a first boundary of the first n-well, and wherein the first distance is selected to provide approximately a desired breakover voltage between the first n-plug and the p-type semiconductor substrate;

forming a second n-plug within the p-type semiconductor substrate; and

forming an isolation structure between the first and second n-plugs.

47. (Amended) The method of claim 46, wherein forming the isolation structure comprises forming at least one of a LOCOS oxide and a surface trench filled with an oxide.

48. (Amended) The method of claim 46, wherein forming an isolation structure comprises forming a gate terminal.

50. (Amended) The method of claim 46, further comprising forming a conductor layer above at least a portion of the first and second n-plugs.

51. (Amended) A method for forming an integrated circuit device, comprising:

providing a semiconductor substrate;

forming a first doped region in the semiconductor substrate;

forming a first doped well within the first doped region;

forming a first doped plug at a first distance from a first boundary of the first doped well, wherein the first distance is selected to provide approximately a first desired breakover voltage between the first doped plug and the first doped region;

forming a second doped plug within the first doped region;

forming an isolation structure between the first and second doped plugs;

forming a bond pad on the semiconductor substrate;

forming a voltage source node on the semiconductor substrate;

coupling the first doped plug to the bond pad;

coupling the second doped plug to the voltage source node; and

forming at least one integrated circuit component on said semiconductor substrate coupled to the bond pad.

REMARKS

In a Request for Filing Divisional Application dated August 20, 2001, claims 1-34 of the parent application (Serial No. 09/310,288) were cancelled. In a Preliminary Amendment dated August 20, 2001, claim 35 was amended and new claims 44-54 were added. Thus, claims 35-54 are pending in the present application.

To present the claims in better form for appeal, Applicant proposes amending the claims as follows. First, Applicant proposes canceling claims 35 and 44. Second, Applicant proposes rewriting dependent claims 37 and 46 in independent form including the limitations set forth in the base claims 35 and 44, and amending claims 36-37 and 45-46 so as to more clearly define the claimed invention. Third, Applicant proposes amending independent claim 51 to include limitations previously set forth in other dependent claims, as well as to more clearly define the